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EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/782,697	BASOL ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,16-21 and 25-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,16-21 and 25-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/26/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's Amendment and RCE filed September 26, 2007. Claims 1-10,16-21,25-26,27-34 are pending, in which claims 27-34 have been newly added. Claims 11-15 and 22-24 were cancelled by Applicant.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

1. Claims 1-5,7-9,16-19,21,27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hongo et al (6,615,854) taken with Collins (2004/0038052) and Nogami (2001/0041447).

Re claim 1, Hongo teaches (at Figs 8,7; col 4, lines 50-57; Figs 2,1; col 1, lines 19-45) a method of forming a layer of a conductive material on a wafer, wherein a seed layer coats a front surface and an edge surface of the wafer, and wherein the edge surface includes a back edge surface, a bevel surface and a front edge surface, the method comprising the steps of: removing an edge portion of the seed layer 83 from the back edge surface and the bevel surface without removing the seed layer form a central portion of the front surface and front edge surface; and forming the conductive material 85 onto the seed layer 83 coating the front edge surface and the front surface of the wafer (Figs 8,7; col 4, lines 50-57; Figs 2,1; col 1, lines 19-45). Re claim 16, Hongo teaches (at Figs 8,7; col 4, lines 50-57; Figs 2,1; col 1, lines 19-45) a method of forming a layer of a conductive material 85 on a wafer comprising a front surface, a back surface and an edge surface, the edge surface including a back edge surface, a bevel surface and a front edge surface, the method comprising the steps of: depositing a seed layer 83 on the front surface and the edge surface of the wafer; removing the seed layer 83 from the back edge surface and the bevel surface; and forming the layer by depositing the conductive material 85 onto the seed layer coating the front edge surface and the front surface (Figs 8,7; col 4, lines 50-57; Figs 2,1; col 1, lines 19-45). Re claims 2,17, wherein, as shown in Figs 8,7, removing at least a part of the seed layer 83 from the front edge surface. Re claims 3,18, wherein the wafer is rotated during removing the edge portion of the seed layer 83 (Figs 3,7-8; col 2, line 63 through col 4). Re claims 4,19, applying a process solution is applied onto the back edge surface of the wafer while it is rotated (Fig 3; col 3, line 3 through col 4). Re claims 5,21, wherein the step of

removing comprises chemical etching (Figs 7-8,3; col 4, lines 50 through col 5, line 12; col 3, line 45 through col 4). Re claim 7, the wafer is rotated prior to removing the at least a part of the seed layer 83 from the front edge surface (Figs 3,7-8; col 3, lines 3-45; col 2, line 63 through col 4). Re claim 8, wherein a process solution is applied to the at least a part of the seed layer on the front edge surface while the wafer is rotated (Figs 3,7,8; col 3, line 3 through col 4, line 67). Re claim 9, wherein the step of removing the at least a part of the seed layer from the front edge surface comprises chemical etching (Figs 7-8,3; col 4, lines 50 through col 5, line 12; col 3, line 45 through col 4). Re claim 27, wherein forming the conductive material 85 includes contacting the seed layer 83 on the front surface or the front edge surface of the wafer W (Figs 1,2,7-8). Re claim 28, wherein removing the edge portion of the seed layer comprising holding the wafer with a wafer carrier (Figs 3-4, col 3, line 3 through col 4), and wherein forming of the layer comprises holding the wafer with the wafer carrier by using the same apparatus (col 5, lines 14-55; Figs 10-11). Re claim 29, wherein chemical etching comprises directing an etching solution towards the back edge of the wafer (Figs 3-5,7-8; col 4, lines 50 through col 5, line 12; col 3, line 45 through col 4).

Re claim 1, Hongo teaches removing the seed layer 83 from the back edge surface and the bevel after forming the conductive material 85 onto the seed layer 83, whereas, claim 1 recites removing the seed layer from the back edge surface and the bevel surface before forming the conductive material, thereby the central portion of the seed layer is exposed, while claim 16 recites the entire seed layer is exposed.

However, Collins teaches (at Figs 2B-2C,3; paragraphs 21-28,11-13) removing of the seed layer 120 (Fig 2B) from the edge surface including the bevel surface, the back edge surface, and part of the front edge surface so as to leave the seed layer 120 (Fig 2C) on the front surface of the wafer (Fig 2C), without removing the seed layer 120 from a central portion of the front surface and front edge surface while the central portion of the seed layer 120 is exposed (Figs 2B-2C), wherein the entire seed layer 120 is exposed (Figs 2B-2C); and then forming the conductive material onto the seed layer 120 coating the front edge surfaces and the front surface of the wafer after removing of the seed layer 120 (Fig 2B) from the edge surface including the bevel surface, the back edge surface, and part of the front edge surface so as to leave the seed

layer 120 (Fig 2C) on the front surface of the wafer (Fig 2C), and contacting the seed layer on the front edge surface of the wafer. Nogami teaches (at Figs (2A-2C) removing of the barrier/seed layer (Figs 2A-2C; paragraphs 17-21) from the edge surface including the bevel surface, the back edge surface, and part of the front edge surface so as to leave the seed/barrier layer on the front surface of the wafer (Fig 2C), without removing the seed layer 116 from a central portion of the front surface and front edge surface while the central portion of the seed layer 116 is exposed (Fig 2B), and wherein the entire seed layer 116 is exposed (Fig 2B); and then forming a conductive material on the seed/barrier layer 116,114 after removing of the seed/barrier layer 116/114 (Figs 2A-2C; paragraphs 17-21) from the edge surface including the bevel surface, the back edge surface, and part of the front edge surface.

Therefore, the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made to forming the conductive material on the seed layer of Hongo after removing the seed layer from the edge surface including the bevel surface, the back edge surface, and part of the front edge surface so as to leave the seed layer on the front surface of the wafer, without removing the seed layer from a central portion of the front surface and front edge surface while the central portion of the seed layer is exposed, as taught by Collins and Nogami. This is because of the desirability to prevent forming the conductive material at unwanted edge surface, and because of the desirability to deposit the conductive material at a selected portion on the seed layer at the front surface of the wafer so that the step of removing the conductive material at the edge surfaces after depositing the conductive material is not necessarily needed, thereby reducing processing steps. This is also because of the desirability to provide copper interconnects with reduced contamination due to copper deposited at the edge or rear of the substrate (Nogami, paragraphs 21,20).

2. Claims 6,10,20,30-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hongo et al (6,615,854) taken with Collins (2004/0038052) and Nogami (2001/0041447), as applied to claims 1-5,7-9,16-19,21,27-29 above, and further of Volodarsky et al (6,352,623).

Hongo, Collins and Nogami teach a method for forming a conductive layer as applied to claims 1-5,7-9,16-19,21,27-29 above.

The references including Hongo already teaches removing the seed layer by chemical etching, wherein the edge of the wafer is inserted into a cavity (Figs 4-5, re claim 33).

Claims 6,10 and 20 recite removing the seed layer by electrochemical etching, and by contacting the wafer with porous media (re claim 32), and rotating the wafer (claim 34).

However, Volodarsky teaches (at Figs 1-2; col 5, lines 8-27, col 4) employing an ECMD process and apparatus for depositing and removing a layer by electrochemical etching or chemical etching, wherein the electrochemical etching comprises contacting the wafer with porous media pad 24 (Fig 1, col 4, lines 45-67, re further claim 32), and wherein the wafer is rotated (Fig 1, col 4, lines 28-67, re claim 34) up to 200 rpm (col 8, lines 13-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the layer of Hongo by employing the ECMD process for removing a layer by electrochemical etching or chemical etching as taught by Volodarsky. This is because electrochemical etching and chemical etching are alternative and art recognized equivalent etching process for removing a portion of the layer from the wafer, wherein the electrochemical etching is an effective process for removing a layer in a reliable manner.

Re claims 30-31, Volodarsky teaches (at col 8, lines 13-25; Fig 1, col 4, lines 28-67) rotating the wafer up to 200 rpm during the etching. Therefore, the subject matter as a whole would have been obvious to one or ordinary skill in the art at the time the invention was made to select the portion of the prior art's range of rotation of the wafer, as taught by Volodarsky, which is within the range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the best results, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948); *In Re Swanson* 56 USPQ 372 (CCPA 1942); *In Re Sola* 25 USPQ 433 (CCPA 1935); and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934).

3. Claims 25,26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hongo et al (6,615,854) taken with Collins (2004/0038052) and Nogami (2001/0041447), as applied to claims 1-5,7-9,16-19,21,27-29 above, and further of Ulrich et al (5,897,379).

Hongo, Collins and Nogami teach a method for forming a conductive layer as applied to claims 1-5,7-9,16-19,21,27-29 above.

Claims 25-26 recite removing at least part of the seed layer from the front edge surface after forming the conductive material layer.

However, Hongo teaches (at Figs 7-8; col 4, line 50 through col 6) removing at least part of the seed layer from the front edge surface after forming the conductive material layer 85. Ulrich also teaches (at Figs 3-5; col 5, line 56 through col 6; Figs 9-11; col 7, lines 22-50; cols 1-2) patterning and removing at least a part of a portion of the conductive layer 32 after forming the conductive material layer 32 in order to form interconnect lines for the integrated circuit (IC).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to continue the semiconductor fabrication of the references including Hongo by patterning and removing a portion of the conductive material layer and a part of the seed layer after forming the conductive material layer, as taught by Ulrich and Hongo. This is because of the desirability to remove the unwanted conductive material layer from the perimeter of the wafer, and because of the desirability to pattern the conductive material layer in order to form an electrical interconnection for an semiconductor device.

Response to Amendment

4. Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Applicant mainly remarked about the claimed invention of removing an edge portion of the seed layer while the central portion of the seed layer is exposed (claim 1) or the entire seed layer is exposed.

In response, it is noted and found unconvincing. Collins and Nogami clearly teaches removing an edge portion of the seed layer while the central portion of the seed layer or the

entire seed layer is exposed, since the removing the edge portion is performed before forming a conductive layer on the seed layer. Applicant appears to argue against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (571) 273-8300.

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Oacs-24-1

Michael Trinh
Primary Examiner